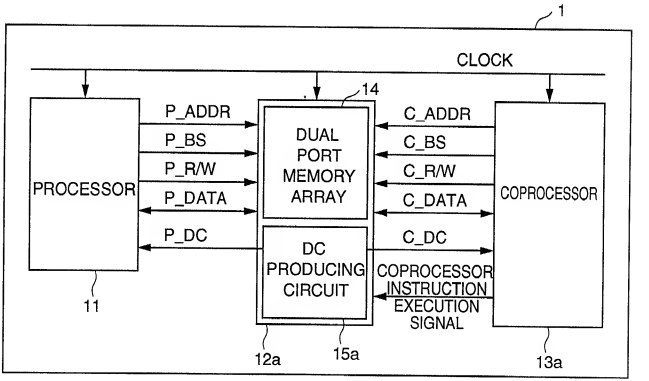


FIG. 1

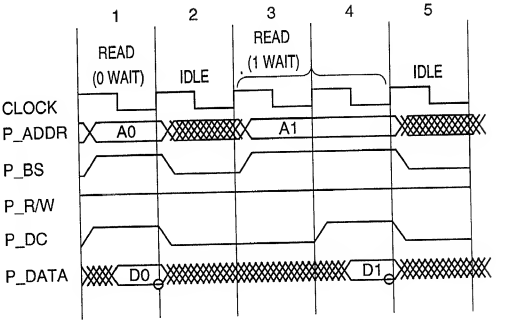


FIG. 2

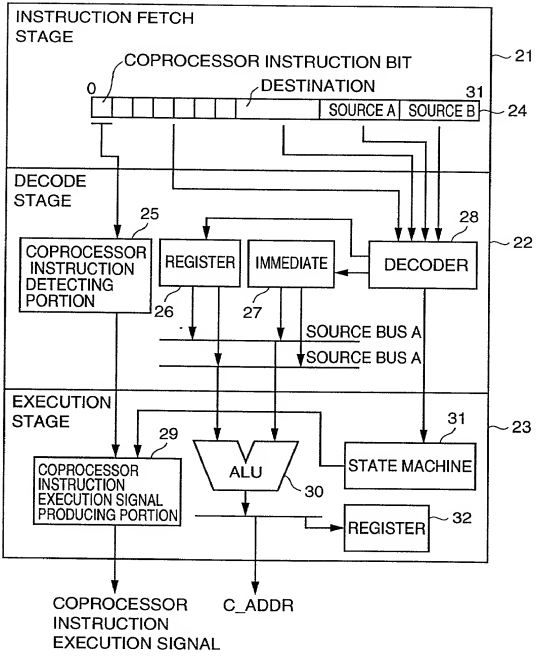
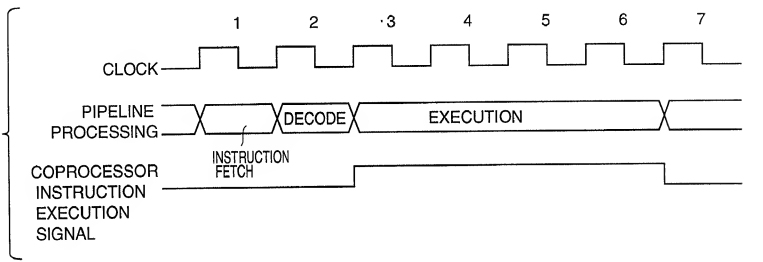

INSTRUCTION FETCH STAGE
COPROCESSOR INSTRUCTION BIT
21
0
DESTINATION
31
SOURCE A
SOURCE B
24
DECODE STAGE
25
28
22
COPROCESSOR INSTRUCTION DETECTING PORTION
REGISTER
IMMEDIATE
DECODER
26
27
SOURCE BUS A
SOURCE BUS A
EXECUTION STAGE
31
23
29
ALU
STATE MACHINE
COPROCESSOR INSTRUCTION EXECUTION SIGNAL PRODUCING PORTION
30
REGISTER
32
COPROCESSOR INSTRUCTION EXECUTION SIGNAL
C_ADDR

FIG. 3

FIG. 4



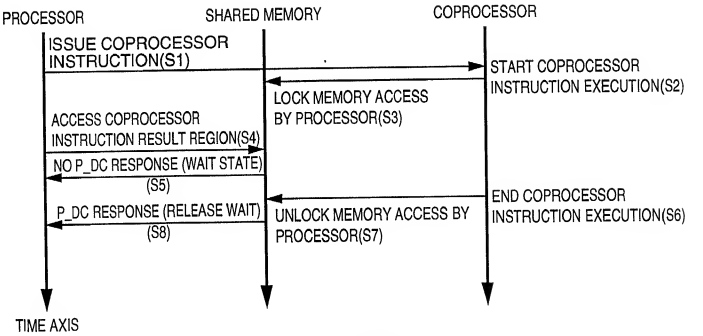


FIG. 5

FIG. 6

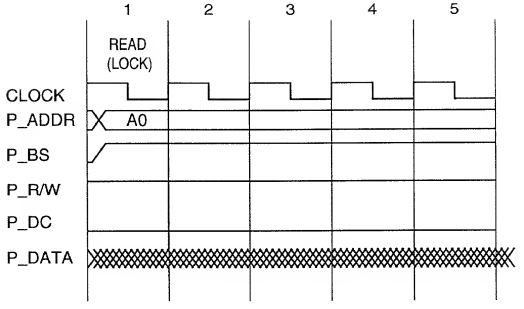
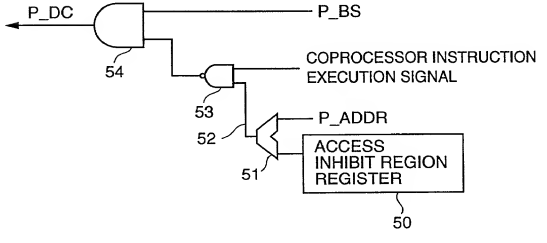

1
2
3
4
5
READ
(LOCK)
CLOCK
P_ADDR
A0
P_BS
P_R/W
P_DC
P_DATA

FIG. 7


P_DC
P_BS
54
COPROCESSOR INSTRUCTION
EXECUTION SIGNAL
53
P_ADDR
52
ACCESS
INHIBIT REGION
REGISTER
51
50

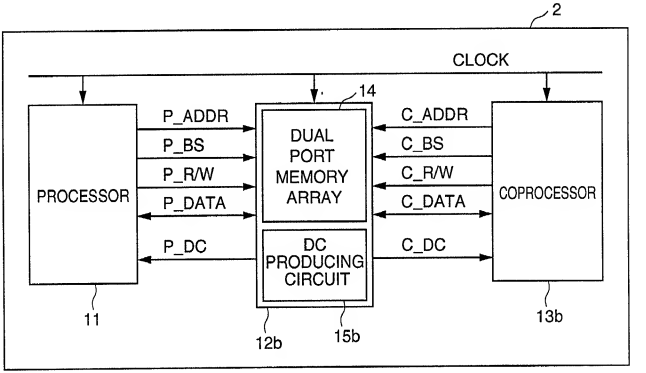


FIG. 8

FIG. 9

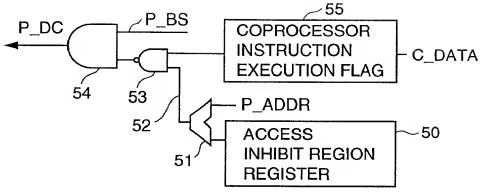
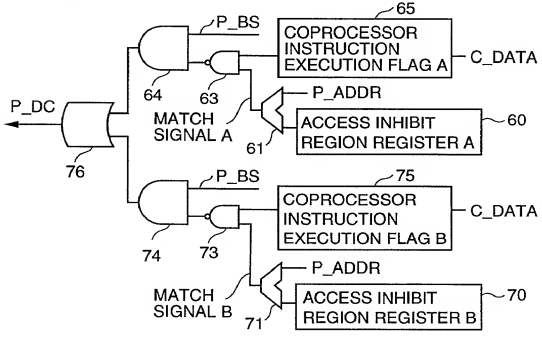

P_DC
P_BS
55
COPROCESSOR INSTRUCTION EXECUTION FLAG
C_DATA
54
53
P_ADDR
52
ACCESS INHIBIT REGION REGISTER
50
51

FIG. 10


65
P_BS
COPROCESSOR INSTRUCTION EXECUTION FLAG A
C_DATA
64
63
P_ADDR
P_DC
MATCH SIGNAL A
ACCESS INHIBIT REGION REGISTER A
60
61
76
75
P_BS
COPROCESSOR INSTRUCTION EXECUTION FLAG B
C_DATA
74
73
P_ADDR
MATCH SIGNAL B
ACCESS INHIBIT REGION REGISTER B
70
71

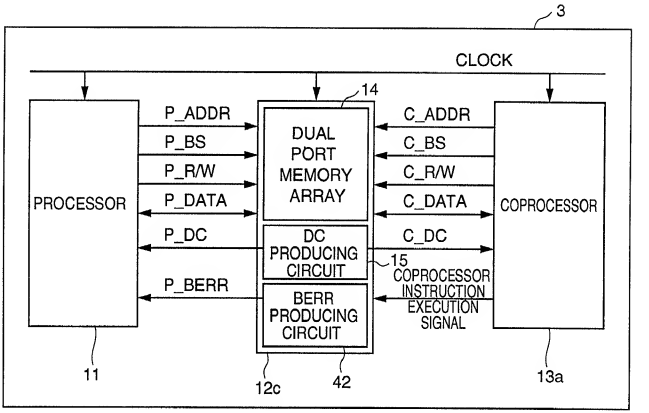


FIG. 11

FIG. 12

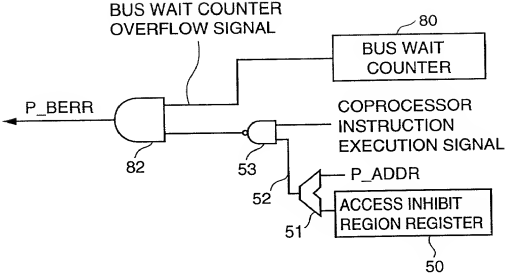
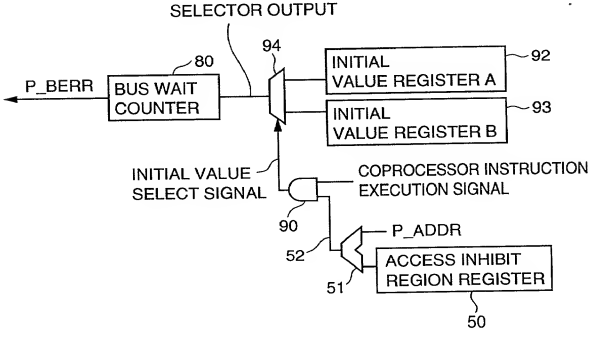

BUS WAIT COUNTER
OVERFLOW SIGNAL
80
BUS WAIT
COUNTER
P_BERR
COPROCESSOR
INSTRUCTION
EXECUTION SIGNAL
82
53
P_ADDR
52
ACCESS INHIBIT
REGION REGISTER
51
50

FIG. 13


SELECTOR OUTPUT
94
80
INITIAL
VALUE REGISTER A
92
P_BERR
BUS WAIT
COUNTER
INITIAL
VALUE REGISTER B
93
INITIAL VALUE
SELECT SIGNAL
COPROCESSOR INSTRUCTION
EXECUTION SIGNAL
90
P_ADDR
52
ACCESS INHIBIT
REGION REGISTER
51
50

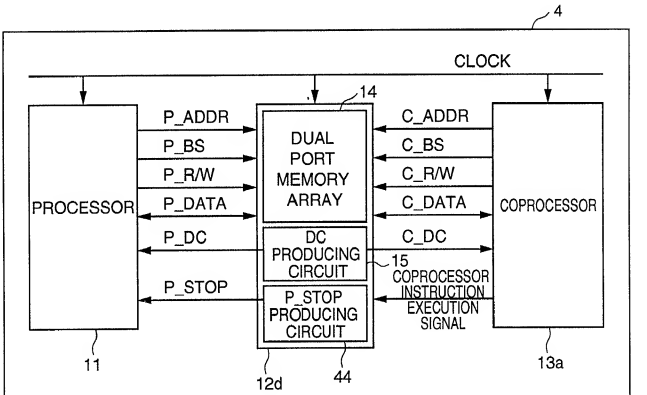


FIG. 14

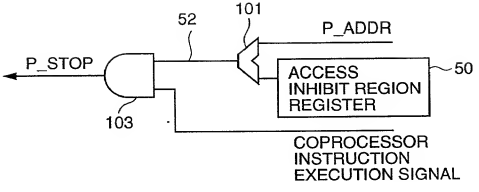


FIG. 15

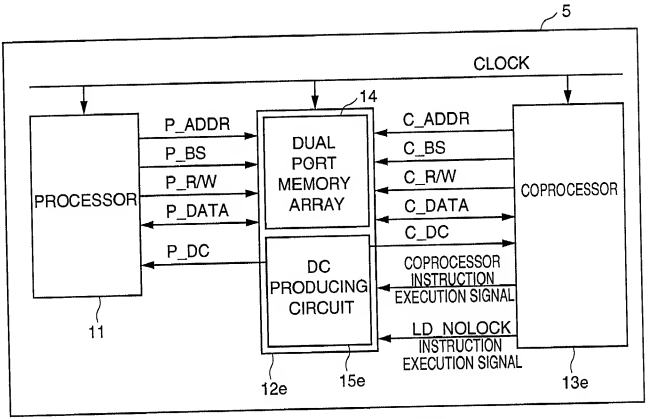


FIG. 16

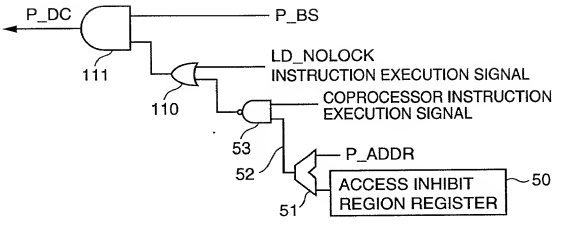

P_DC
P_BS
111
LD_NOLOCK
INSTRUCTION EXECUTION SIGNAL
110
COPROCESSOR INSTRUCTION
EXECUTION SIGNAL
53
P_ADDR
52
ACCESS INHIBIT
REGION REGISTER
50
51

FIG. 17

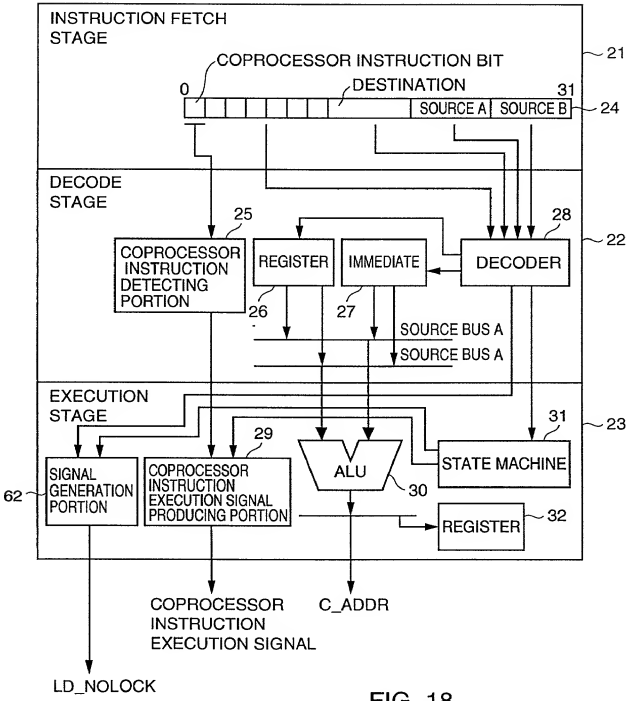

INSTRUCTION FETCH STAGE
COPROCESSOR INSTRUCTION BIT
21
0
DESTINATION
31
SOURCE A
SOURCE B
24
DECODE STAGE
25
28
22
COPROCESSOR INSTRUCTION DETECTING PORTION
REGISTER
IMMEDIATE
DECODER
26
27
SOURCE BUS A
SOURCE BUS A
EXECUTION STAGE
31
23
29
ALU
STATE MACHINE
62
SIGNAL GENERATION PORTION
COPROCESSOR INSTRUCTION EXECUTION SIGNAL PRODUCING PORTION
30
REGISTER
32
COPROCESSOR INSTRUCTION EXECUTION SIGNAL
C_ADDR
LD_NOLOCK

FIG. 18